

WHAT IS CLAIMED:

1. A transceiver couplable to a communications network
2 having a jitter control processor with a transmitter stage, said
3 transmitter stage configured to control a transmit signal,
4 comprising:

5 a transmit time error measurement system configured to
6 generate a transmit time error signal as a function of timing
7 synchronization associated with a communications network clock and
8 a transceiver master clock;

9 a transmit filter circuit configured to develop a filtered
10 time error signal as a function of said transmit time error signal;
11 and

12 a stuffing control system configured to insert a stuffing
13 control signal into said transmit signal as a function of said
14 transmit time error signal and said filtered time error signal.

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3. The transmitter stage as recited in Claim 1 wherein said
2 transmit filter stage comprises a two-input summing node,
3 coefficient elements and a three-input summing node.

4. The transmitter stage as recited in Claim 1 wherein said
2 transmit filter stage comprises a delay element.

5. The transmitter stage as recited in Claim 1 wherein said
2 stuffing control signal includes a maximum of four bits.

6. A method of operating a transceiver couplable to a
2 communications network having a jitter control processor with a
3 transmitter stage, comprising:

4 generating a transmit time error signal as a function of
5 timing synchronization associated with a communications network
6 clock and a transceiver master clock;

7 filtering said transmit time error signal to develop a
8 filtered time error signal; and

9 providing a stuffing control signal into a transmit signal as
10 a function of said transmit time error signal and said filtered
11 time error signal.

7. The method as recited in Claim 6 further comprising
2 reducing a communications network clock signal to a transmitter
3 stage frame rate.

8. The method as recited in Claim 6 wherein said filtering
2 is performed by a transmit filter stage comprising a two-input
3 summing node, coefficient elements and a three-input summing node.

9. The method as recited in Claim 6 wherein said filtering
2 is performed by a transmit filter stage comprising a delay element.

10. The method as recited in Claim 6 wherein said stuffing
2 control signal includes a maximum of four bits.

0000000000000000

11. A transceiver couplable to a communications network
2 having a jitter control processor with a receiver stage, said
3 receiver stage, comprising:

4 a receive time error measurement system configured to generate
5 a receive time error signal as a function of a receive clock signal
6 experiencing jitter and a feedback signal;

7 a jitter processing circuit configured to develop a dejittered
8 control signal as a function of said time error signal; and

9 a clock generator system configured to provide said feedback
10 signal as a function of said dejittered control signal and a
11 transceiver local clock signal.

12. The receiver stage as recited in Claim 11 wherein said
jitter processing circuit comprises a receive filter stage.

13. The receiver stage as recited in Claim 12 wherein said
receive filter stage comprises a summing node and a delay element.

14. The receiver stage as recited in Claim 11 wherein said
2 dejittered control signal comprises a control and offset component.

15. The receiver stage as recited in Claim 11 wherein said
2 clock generator system is configured to provide a dejittered clock
3 signal.

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16. A method of operating a transceiver couplable to a
2 communications network having a jitter control processor with a
3 receiver stage, comprising:

4 generating a receive time error signal as a function of a
5 receive clock signal experiencing jitter and a feedback signal;

6 developing a dejittered control signal as a function of said
7 time error signal; and

8 creating said feedback signal as a function of said dejittered
9 control signal and a transceiver local clock signal.

DETAILED DESCRIPTION

17. The method as recited in Claim 16 wherein said developing
is performed by a jitter processing circuit comprising a receive
filter stage.

18. The method as recited in Claim 17 wherein said receive
filter stage comprises a summing node and a delay element.

19. The method as recited in Claim 16 wherein said dejittered
2 control signal comprises a control and offset component.

20. The method as recited in Claim 16 wherein said creating
2 is performed by a clock generator system that provides a dejittered
3 clock signal.

21. A transceiver coupled to a communications network, comprising:

a system interface that performs system level functions for said transceiver;

a framer that formats signals from said system interface;

a bit pump, coupled to said framer and having a transmit and receive path;

an analog front end, coupled to said bit pump and including a transceiver local clock, that provides a clocking reference for said transceiver; and

a jitter control processor having a transmitter and receiver stage, said transmitter stage configured to control a transmit signal and including:

a transmit time error measurement system that generates a transmit time error signal as a function of timing synchronization associated with a communications network clock and a transceiver master clock,

a transmit filter circuit that develops a filtered time error signal as a function of said transmit time error signal, and

a stuffing control system that inserts a stuffing control signal into said transmit signal as a function of said

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transmit time error signal and said filtered time error signal,

said receiver stage, including:

a receive time error measurement system that generates a receive time error signal as a function of a receive clock signal experiencing jitter and a feedback signal,

a jitter processing circuit that develops a dejittered control signal as a function of said time error signal, and

a clock generator system that provides said feedback signal as a function of said dejittered control signal and said transceiver local clock signal.

22. The transceiver as recited in Claim 21 wherein said transmitter stage further comprises a division counter that reduces a communications network clock signal to a transmitter stage frame rate.

23. The transceiver as recited in Claim 21 wherein said
3 transmit filter stage comprises a two-input summing node,
coefficient elements and a three-input summing node.

24. The transceiver as recited in Claim 21 wherein said
2 transmit filter stage comprises a delay element.

25. The transceiver as recited in Claim 21 wherein said
2 stuffing control signal includes a maximum of four bits.

26. The transceiver as recited in Claim 21 wherein said
2 jitter processing circuit comprises a receive filter stage.

27. The transceiver as recited in Claim 26 wherein said
2 receive filter stage comprises a summing node and a delay element.

28. The transceiver as recited in Claim 21 wherein said
dejittered control signal comprises a control and offset component.

29. The transceiver as recited in Claim 21 wherein said clock
generator system provides a dejittered clock signal.

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